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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/571,426	03/10/2006	Mitsuyoshi Mori	071971-0494	3460

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EXAMINER	
NICELY, JOSEPH C	
ART UNIT	PAPER NUMBER
2813	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/571,426	MORI ET AL.	
	Examiner	Art Unit	
	Joseph C. Nicely	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/10/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-11 are presented for examination.

Claim Objections

2. Claim 1 is objected to because of the following informalities: "imaging apparatus comprising" should read –imaging apparatus comprising:–. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Examiner notes that a machine translation of JP-2004-172394 is used in the following rejections as an English language equivalent. A copy of a human translation of JP-2004-172394 will be placed in IFW when it is made available to the Examiner.

6. Claims 1, 2, 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomohisa (JP-2004-172394 and Tomohisa hereinafter).

As to claim 1: Tomohisa discloses **a solid state imaging apparatus** ([0015], line 1; solid state image sensor) **comprising: a photoelectric conversion section** (PD, photodiode is photoelectric conversion section) **formed in an imaging area** (100A) **of a substrate** (Fig. 2; [0017]; substrate 1)**, and an isolation region** (9, trench separation field) **formed in at least one part of the silicon substrate located around the photoelectric conversion section** (isolation region 9 is formed in the pixel region PXL and the region 9 surrounds the photoelectric conversion section PD so as to provide separation) **and made of an isolation material having a thermal expansion coefficient larger than silicon oxide and equal to or smaller than silicon** (Fig. 2; [0017] and [0026]; isolation region 9 is filled with polysilicon, which has a thermal expansion coefficient larger than silicon oxide and equal to or smaller than silicon)**.**

Tomohisa fails to expressly disclose where the substrate is a **silicon substrate**. However, the claim would have been obvious to a person having ordinary skill in the art at the time the invention was made since the use of silicon as the material comprising a substrate was well known in the art and within the ordinary capabilities of one skilled in the art.

7. As to claim 2: Tomohisa discloses **where the isolation region** (9, trench separation field) **is made of the isolation material** (polysilicon 10c) **with which an isolation trench** (slot of the trench separation field 9) **is filled** (Fig. 2; [0017]-[0018]; isolation material 10c substantially fills the isolation trench that is formed through

anisotropic etching)**, said isolation trench** (slot of trench separation field 9) **being formed in at least one part of the silicon substrate located around the photoelectric conversion section** (Fig. 2; [0017]-[0018]; isolation trench (slot of trench isolation separation field 9) if formed to surround the photoelectric conversion section PD in the PXL region)**.**

8. As to claim 4: Tomohisa discloses **an impurity-doped semiconductor layer** (diffusion zone 9a) **formed in a region of the silicon substrate forming the bottom and sidewalls of the isolation trench** (slot of trench isolation separation field 9) **by doping the region with an impurity** (Fig. 2; [0018]; step 4, polysilicon 10c, which is doped with boron, is annealed which causes doping (through diffusion) of the boron into the walls (i.e., bottom surface and sidewalls) of the trench)**.**

9. As to claim 5: Tomohisa discloses **where the isolation material is silicon** ([0017]; isolation material 10c is comprised of a type of silicon, polysilicon)**.**

10. As to claim 6: Tomohisa discloses **a MOS transistor** (Qt) **formed in the imaging area** (Figs. 2 and 4; [0029]; Qt in Fig. 2 corresponds to 37 (gate oxide) and 35 (gate electrode) in Fig. 4)**.**

Tomohisa fails to expressly disclose **where the isolation material contains an impurity of the opposite conductivity type to source and drain regions of the MOS transistor.** However, the claim would have been obvious to a person having ordinary skill in the art at the time the invention was made since, as stated in KSR Int'l v. Teleflex Inc., 127 S. Ct., 1727 (2007), a person of ordinary skill has good reason to pursue the known options within his or her technical grasp (i.e., there are two main types of

conductivity–p or n–). If this leads to the anticipated success (e.g. a desired output from the device), it is likely the product not of innovation but of ordinary skill and common sense.

11. As to claim 7: Tomohisa discloses **where the isolation material is made of amorphous silicon, polycrystalline silicon or porous silicon** ([0017]; isolation material 10c is comprised of polysilicon, i.e., polycrystalline silicon)**.**

12. As to claim 11: Tomohisa fails to expressly disclose **a camera comprising the solid state imaging apparatus according to Claim 1.** However, the claim would have been obvious to a person having ordinary skill in the art at the time the invention was made since, as stated in KSR Int'l v. Teleflex Inc., 127 S. Ct., 1727 (2007), the combination of familiar elements (e.g. a solid state imaging apparatus or sensor such as disclosed in claim 1 and a camera that uses a solid state imaging apparatus or sensor) according to known methods is likely to be obvious when it does no more than yield predictable results (e.g. a digital camera).

13. Claims 3 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomohisa as applied to claim 1 above, and further in view of Inoue (US 6,964,905 and Inoue hereinafter).

As to claim 3: Although the structure disclosed by Tomohisa shows substantial features of the claimed invention (discussed in paragraphs 6-7 above), it fails to expressly disclose:

an insulating film covering the bottom and sidewalls of the isolation trench.

Nonetheless, this feature is well known in the art and would have been an obvious modification of the structure disclosed by Tomohisa, as evidenced by Inoue.

Inoue discloses a trench isolation region having:

an insulating film covering the bottom and sidewalls of the isolation trench (Fig. 4, No. 6; col. 4, lines 30-39)**.**

Given the teachings of Inoue, a person having ordinary skill in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Tomohisa by employing the well known or conventional features of trench formation, such as displayed by Inoue, by employing a liner layer for a trench isolation region in order to prevent oxidation of the inner wall.

14. As to claim 8: Tomohisa discloses **a method for fabricating a solid state imaging** ([0015], line 1; solid state image sensor) **apparatus, said method comprising the steps of: forming an isolation trench by etching a region of a substrate** (Fig. 2; [0018]; isolation trench is the slot of the trench separation field 9)**; filling the isolation trench with a silicon layer** (Fig. 2; [0018]; the silicon layer filling the isolation trench is polysilicon 10c)**.**

Tomohisa fails to expressly disclose where the substrate is a **silicon substrate**. However, the claim would have been obvious to a person having ordinary skill in the art at the time the invention was made since the use of silicon as the material comprising a substrate was well known in the art and within the ordinary capabilities of one skilled in the art.

Tomohisa fails to expressly disclose **and implanting an impurity into a predetermined region of the silicon layer.** Tomohisa in [0017] only states that the polysilicon layer (silicon layer) contains boron. The claim would have been obvious to a person having ordinary skill in the art at the time the invention was made since, as stated in KSR Int'l v. Teleflex Inc., 127 S. Ct., 1727 (2007), a person of ordinary skill has good reason to pursue the known options within his or her technical grasp (i.e., doping a layer, such as polysilicon or silicon, through ion implantation or diffusion). If this leads to the anticipated success (e.g. a desired output from the device), it is likely the product not of innovation but of ordinary skill and common sense.

Furthermore, Tomohisa fails to expressly disclose **forming an insulating film to cover the bottom and sidewalls of the isolation trench** before the filling of the isolation trench with a silicon layer**.**

In the same field of endeavor, Inoue discloses a method **forming an insulating film to cover the bottom and sidewalls of the isolation trench** (Fig. 4, No. 6; col. 4, lines 30-39) before the filling of the isolation trench with a silicon layer**.**

Given the teachings of Inoue, a person having ordinary skill in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Tomohisa by employing the well known or conventional features of trench formation, such as displayed by Inoue, by employing a liner layer for a trench isolation region in order to prevent oxidation of the inner wall.

15. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomohisa in view of Inoue as applied to claim 8 above, and further in view of Lee (US 2004/0127035 and Lee hereinafter).

As to claim 9: Although the structure disclosed by Tomohisa in view of Inoue shows substantial features of the claimed invention (discussed in paragraph 14 above), it fails to expressly disclose:

further comprising the step of making the silicon layer porous.

Nonetheless, this feature is well known in the art and would have been an obvious modification of the structure disclosed by Tomohisa in view of Inoue, as evidenced by Lee.

Lee discloses a method for forming an isolation film having:

further comprising the step of making the silicon layer porous ([0028], lines 9-11).

The claim would have been obvious to a person having ordinary skill in the art at the time the invention was made since, as stated in KSR Int'l v. Teleflex Inc., 127 S. Ct., 1727 (2007), the combination of familiar elements (e.g. having a silicon layer on a substrate and forming a porous silicon film therefrom) according to known methods (e.g. electrochemical etch process) is likely to be obvious when it does no more than yield predictable results (e.g. a trench film with desired properties).

16. As to claim 10: Tomohisa combined with Inoue and in view of Lee disclose **attaching an electrode to part of the silicon layer** (Fig. 1; [0011] and [0021]; to apply a voltage to create the work electrode, some component (a preliminary electrode or

electrode) is implicitly attached to the layer/device to create the electrical connection)**; and immersing, in a solution, part of the silicon layer excluding the part thereof to which the electrode is attached and then passing current via the electrode through the silicon layer** (Fig. 1; [0011] and [0021]; Examiner interprets that solution 160 (electrolyte) is formed only on the top surface of the wafer and does not occur in the area underneath the wafer, i.e., the area where the work electrode exists)**.**

The claim would have been obvious to a person having ordinary skill in the art at the time the invention was made since, as stated in KSR Int'l v. Teleflex Inc., 127 S. Ct., 1727 (2007), the combination of familiar elements (e.g. having a silicon layer on a substrate and forming a porous silicon film therefrom) according to known methods (e.g. electrochemical etch process) is likely to be obvious when it does no more than yield predictable results (e.g. a trench film with desired properties).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph C. Nicely whose telephone number is (571) 270-3834. The examiner can normally be reached on Monday through Friday 7:30AM-5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Joseph C. Nicely/
Examiner, Art Unit 2813

/Carl Whitehead Jr./
Supervisory Patent Examiner, Art Unit 2813